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IN THE CLAIMS:

1. (currently amended) A data processing system having a first and a second mode of operation, comprising:

a central processing unit having a first input to receive a first signal wherein a first state of the first signal enables the first mode of operation and a second state of the first signal enables the second mode of operation, wherein:

the first mode of operation utilizes branch prediction; ~~and~~

the second mode of operation utilizes substantially no branch prediction; and

the central processing unit comprises:.

selecting circuitry having a first input for receiving a sequential address, a second input for receiving a target address, and a third input for receiving a control signal to select between the first input and the second input, and an output for providing one of the first input and the second input;

an instruction fetch unit, coupled to the selecting circuitry, having a first output to provide the sequential address and a second output for providing the target address; and

control circuitry, coupled to the selecting circuitry, having a first input to receive the first signal, having a first output to provide the control signal based on the first signal, having a second input to receive a condition signal, and having a third input to receive a branch decode signal, wherein the control signal is based further in part on the condition signal and the branch decode signal.

2. – 3. (cancelled)

4. (currently amended) The data processing system of claim ~~3~~1, wherein the condition signal indicates a condition code calculation and the branch decode signal indicates that a branch instruction is being decoded.

5. (original) The data processing system of claim 4, wherein the central processing unit further comprises:

a decode control unit, coupled to the control circuitry, having an output to provide the branch decode signal; and

an execution unit, coupled to the decode control unit, having an output to provide the condition signal.

6. (original) The data processing system of claim 1, wherein the first signal is hardwired to a predetermined state.

7. (original) The data processing system of claim 1, further comprising a control register having a field corresponding to the first signal, wherein the field is capable of being dynamically programmed.

8. (original) The data processing system of claim 1, wherein the data processing system comprises only the central processing unit.

9. (original) The data processing system of claim 1, wherein:

the first mode of operation results in a first address setup timing; and

the second mode of operation results in a second address setup timing, wherein the first address setup timing allows for an earlier address valid time as compared to the second address setup timing.

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10. (currently amended) A data processing system having a first and a second mode of operation, comprising:

a first input to receive a first signal wherein a first state of the first signal enables the first mode of operation and a second state of the first signal enables the second mode of operation, wherein:

the first mode of operation ~~results in a first address setup timing~~ allows for a first address valid time corresponding to a first driven address, the first address valid time providing a first memory access time within a clock cycle in which the first address is driven; and

the second mode of operation ~~results in a second address setup timing that~~ allows for a second address valid time corresponding to a second driven address, wherein the second address valid time provides additional memory access time, as compared with the first memory access time, within a clock cycle in which the second address is driven. ~~an earlier address valid time as compared to the first address setup timing.~~

11. (original) The data processing system of claim 10, wherein the first address setup timing is realized utilizing a first level of branch prediction, and the second address setup timing is realized utilizing a second level of branch prediction that is more aggressive than the first level of branch prediction.

12. (original) The data processing system of claim 11, wherein the first mode of operation performs substantially no branch predictions.

13. (original) The data processing system of claim 10, wherein the central processing unit comprises:

selecting circuitry having a first input for receiving a sequential address, a second input for receiving a target address, and a third input for receiving a control signal to select between the first input and the second input, and an output for providing one of the first input and the second input;

an instruction fetch unit, coupled to the selecting circuitry, having a first output to provide the sequential address and a second output for providing the target address; and

control circuitry, coupled to the selecting circuitry, having a first input to receive the first signal and having a first output to provide the control signal based on the first signal.

14. (original) The data processing system of claim 10, wherein the first signal is hardwired to a predetermined state.

15. (original) The data processing system of claim 10, further comprising a control register having a field corresponding to the first signal, wherein the field is software programmable.

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16. (currently amended) In a data processing system having a first and a second mode of operation, a method for altering an address setup time comprising:

receiving a first input signal;

if the first input signal has a first state, operating in the first mode of operation, wherein the first mode of operation ~~results in a first address setup timing~~ allows for a first address valid time corresponding to a first driven address, the first address valid time providing a first memory access time within a clock cycle in which the first address is driven;

if the first input signal has a second state, operating in the second mode of operation, wherein the second mode of operation ~~results in a second address setup timing~~ allows for a second address valid time corresponding to a second driven address, wherein the second address valid time provides additional memory access time, as compared with the first memory access time, within a clock cycle in which the second address is driven. ~~having an earlier address valid time as compared to the first address setup timing.~~

17. (original) The method of claim 16, wherein the first mode of operation utilizes a first level of branch prediction and the second mode of operation utilizes a second level of branch prediction.

18. (original) The method of claim 17, wherein the first level is less aggressive than the second level.

19. (original) The method of claim 18, wherein the first level performs substantially no branch predictions.

20. (original) The method of claim 16, wherein operating in the first mode of operation comprises resolving a condition of a branch instruction prior to accessing a target instruction of the branch instruction.